

FIG. 3 - Prior Art

FIG. 4 is a schematic diagram of a memory cell in a prior art device. The memory cell includes a source region 22, a drain region 19, and a bulk region 16. A control gate 10 is positioned over the source region, and an access gate 18 is positioned over the drain region. The memory cell is formed in a substrate 38, which includes a p-well 40, an n-well 41, and a p-substrate 16. The source region 22 is connected to a source terminal 14, and the drain region 19 is connected to a drain terminal 17. The control gate 10 is connected to a control gate terminal 11, and the access gate 18 is connected to an access gate terminal 13. The memory cell is shown in a cross-sectional view, with the source region 22 and drain region 19 separated by a channel region 15. The control gate 10 and access gate 18 are positioned over the channel region 15. The substrate 38 is shown with a p-well 40, an n-well 41, and a p-substrate 16. The source region 22 is formed in the p-well 40, and the drain region 19 is formed in the n-well 41. The channel region 15 is formed in the p-substrate 16. The control gate 10 and access gate 18 are formed in the p-well 40. The memory cell is shown in a cross-sectional view, with the source region 22 and drain region 19 separated by a channel region 15. The control gate 10 and access gate 18 are positioned over the channel region 15. The substrate 38 is shown with a p-well 40, an n-well 41, and a p-substrate 16. The source region 22 is formed in the p-well 40, and the drain region 19 is formed in the n-well 41. The channel region 15 is formed in the p-substrate 16. The control gate 10 and access gate 18 are formed in the p-well 40.

Selected WL                      Non-Selected WL

MODE	Vcg	Vag	Vcg	Vag	Vs	Vd	Vpwell	Vnwell
PROGRAM	-7 TO -11 VOLTS	8 VOLTS	0 VOLTS	0 VOLTS	HIGH Z	5 TO 8 VOLTS	0 VOLTS	3.3 VOLTS
PROGRAM INHIBIT	-7 TO -11 VOLTS	8 VOLTS	0 VOLTS	0 VOLTS	HIGH Z	0 VOLTS	0 VOLTS	3.3 VOLTS
ERASE	8 TO 10 VOLTS	0 VOLTS			-8 TO -10 VOLTS	HIGH Z	8 TO 10 VOLTS	3.3 VOLTS
READ	3.3 VOLTS	3.3 VOLTS	0 VOLTS	0 VOLTS	0 VOLTS	1 VOLT	0 VOLTS	3.3 VOLTS

FIG. 4 - Prior Art

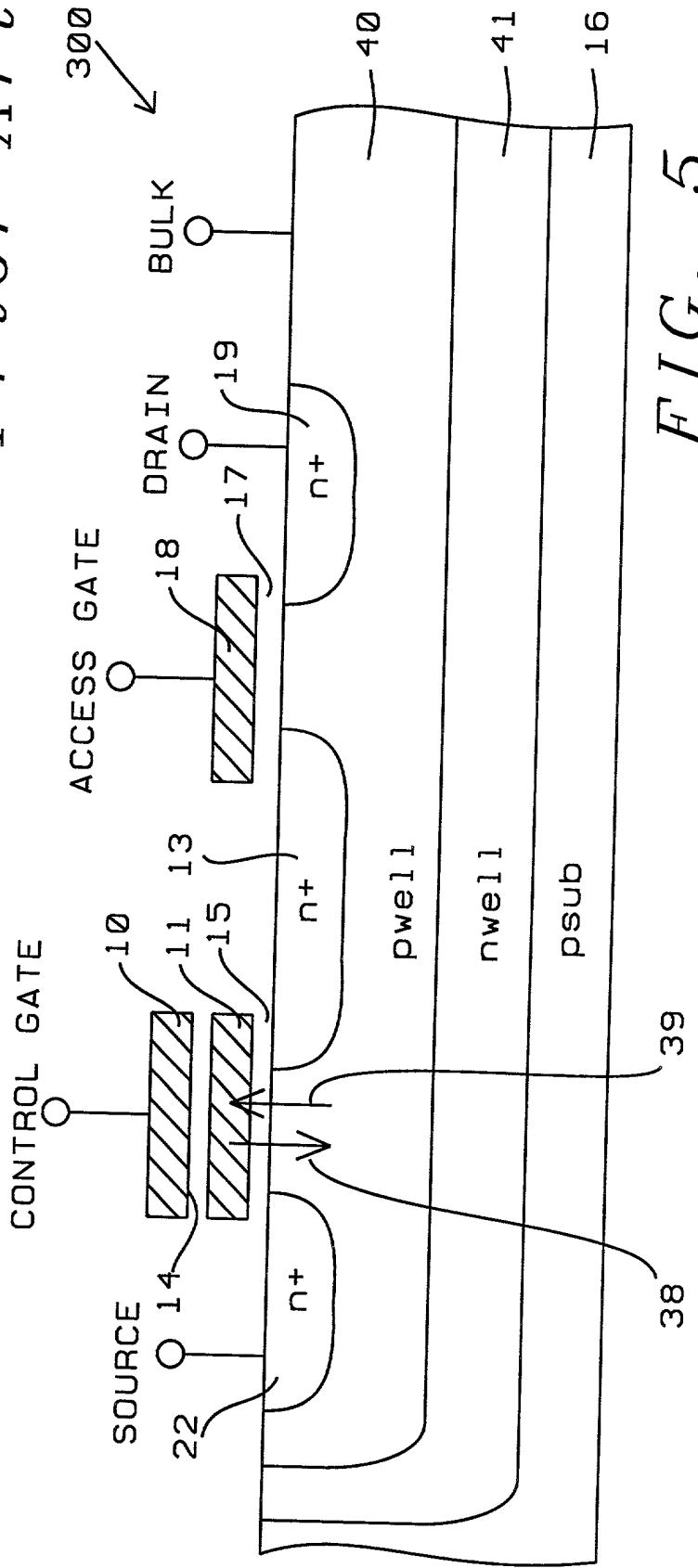


FIG. 5

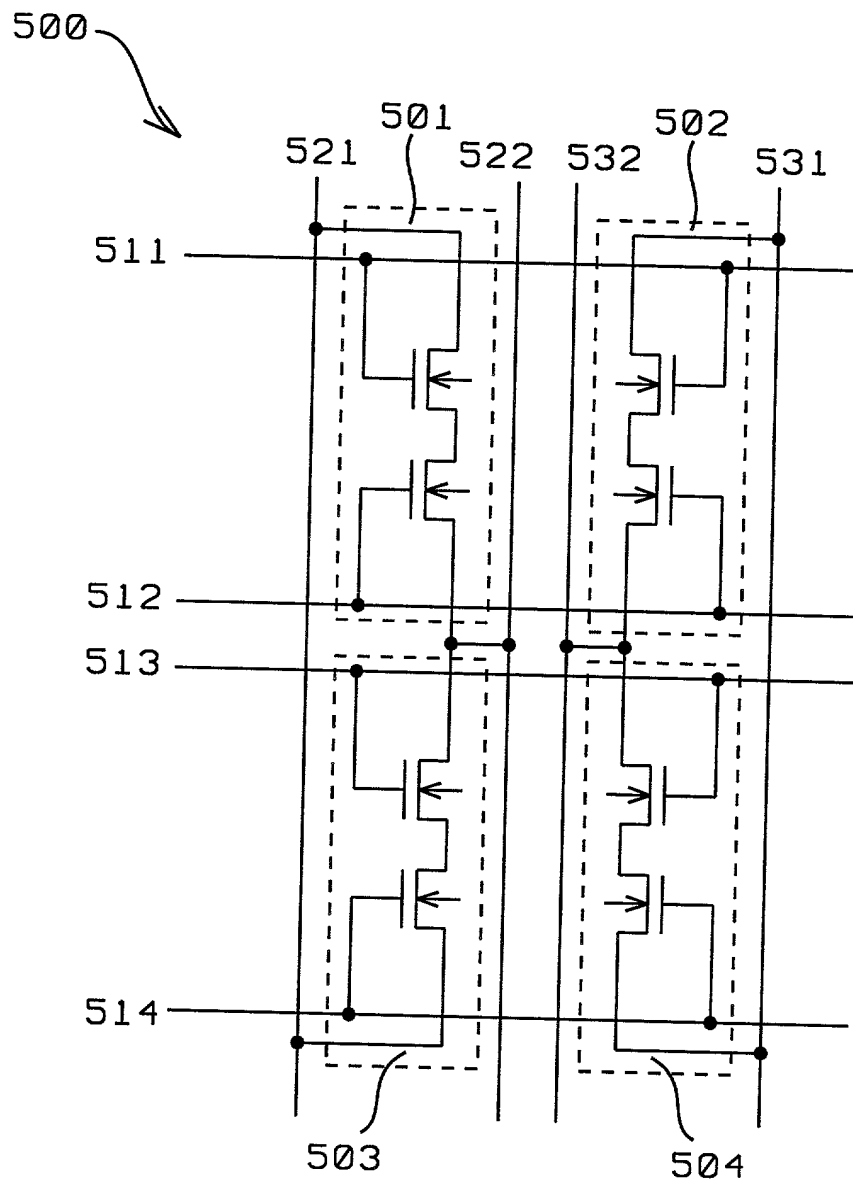


FIG. 6

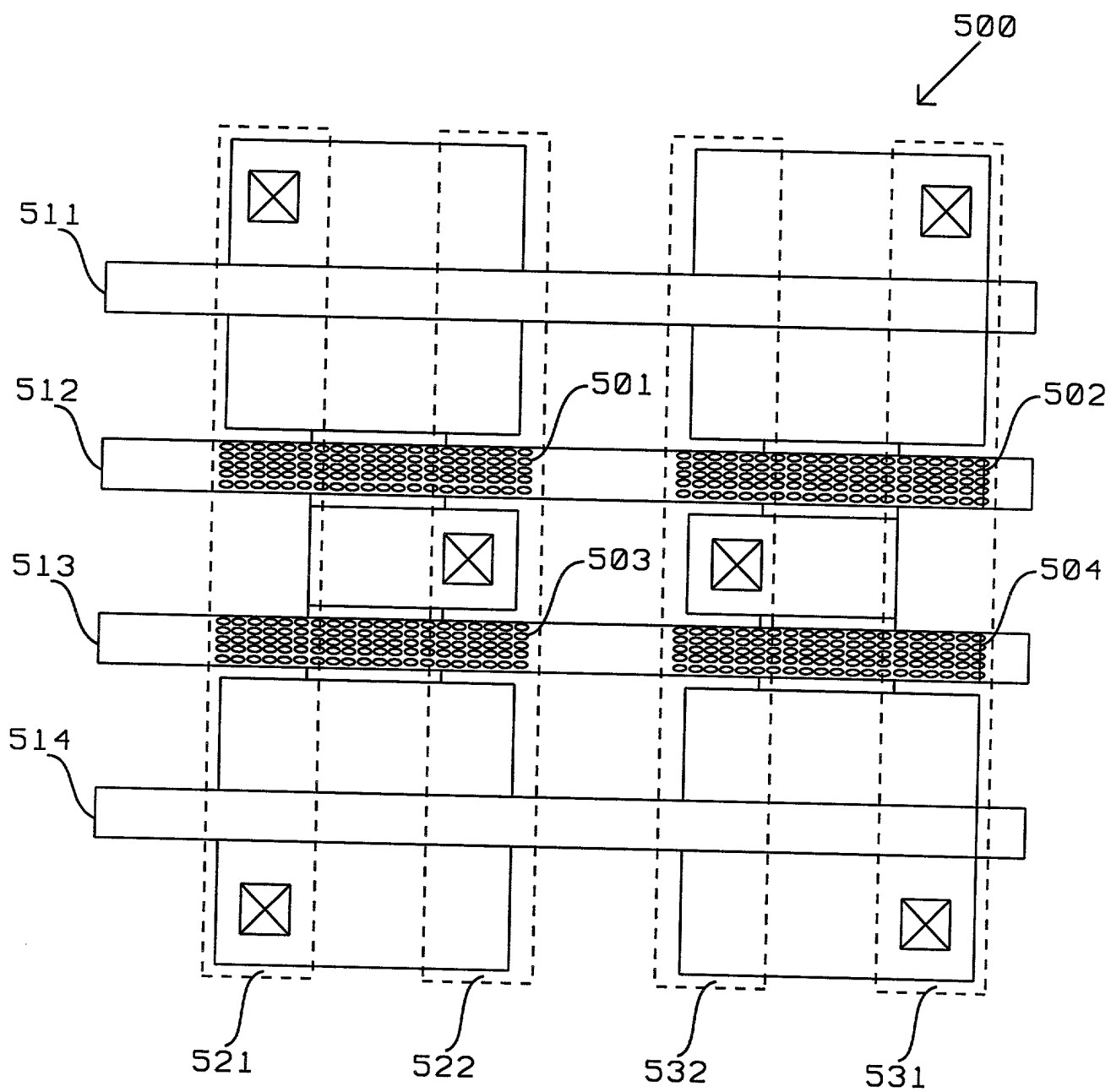


FIG. 7

MODE	Selected WL		Non-Selected WL			
	Vcg	Vag	Vcg	Vag	Vs	Vd
ERASE	-10 VOLTS	0 VOLT	-	-	5 VOLTS	HIGH Z
PROGRAM	Vpgm	Vcc	-2.5 VOLTS	Vcc	HIGH Z	-5 VOLTS
PROGRAM INHIBIT	Vpgm	Vcc	-2.5 VOLTS	Vcc	HIGH Z	-5 VOLTS
READ	Vcc	Vcc	0 VOLTS	0 VOLTS	0 VOLTS	1 VOLT
						0 VOLTS

FIG. 8a

MODE	Selected WL		Non-Selected WL			
	Vcg	Vag	Vcg	Vag	Vs	Vd
ERASE	-15 VOLTS	0 VOLT	-	-	0 VOLTS	HIGH Z
PROGRAM	Vpgm	8 VOLTS	2.5 VOLTS	8 VOLTS	HIGH Z	0 VOLTS
PROGRAM INHIBIT	Vpgm	8 VOLTS	2.5 VOLTS	8 VOLTS	HIGH Z	5 VOLTS
READ	Vcc	Vcc	0 VOLTS	0 VOLTS	0 VOLTS	1 VOLT
						0 VOLTS

FIG. 8b